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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/704,467	ROTH ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005 and 10 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-9,11-16,18-21 and 23-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-9,11-16,18-21 and 23-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/27/03; 3/30/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS 7/5/05*.

DETAILED ACTION

1. Claims 1, 3, 5-9, 11-16, 18-21, and 23-31 have been considered. Claims 1, 9, 12, 13, 16, and 21 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as filed 08 August 2005; Amendment as filed 05 July 2005; IDS (2 pages) as filed 05 July 2005; and Amendment as filed 10 August 2005.

Information Disclosure Statement

3. The information disclosure statement filed 05 July 2005 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because some of the references had been cited in a previous IDS and already considered. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

4. A copy of the IDS citing these references and considered by the Examiner has been provided.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 9, 16, 21, and 29 are rejected under 35 U.S.C. 102(b) as being taught by Edgington et al., U.S. Patent Number 5,530,804.

7. Referring to claim 9, Edgington has taught a method of providing instructions to a processor, the method comprising:

a. Loading a plurality of instructions into an emulation instruction register from a test interface (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; column 5, lines 25-29; column 6, lines 4-25; column 1, line 59 to column 11, line 11; Figure 1; Figure 2; Figure 5; and Figure 6). In regards to Edgington, when the processor is in debug/test/emulator mode, all registers in the processor are used for the emulations instructions and data, so they are emulation registers.

b. Receiving a run-test idle state signal (Edgington column 3, lines 4-29), the run-test idle state signal indicating entry of the test interface into a run-test idle state (Edgington column 3, lines 4-29);

c. Providing the plurality of instructions to the processor in response to the receipt of the run-test idle state signal (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; Figure 1; and Figure 2); and

d. Processing the plurality of instructions without receiving another run-test idle state signal (Edgington column 3, lines 4-29).

8. Referring to claim 16, Edgington has taught a processor comprising:

a. A test interface (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; Figure 1; and Figure 2);

b. An emulation instruction register adapted to store a plurality of emulation instructions received from the test interface (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; column 5, lines 25-29; column 6, lines 4-25; column 1, line 59 to column 11, line 11; Figure 1; Figure 2; Figure 5; and Figure 6). In regards to Edgington, when the processor is in debug/test/emulator mode, all registers in the processor are used for the emulations instructions and data, so they are emulation registers.

c. Emulation control logic adapted to supply the plurality of emulation instructions to a processor pipeline in response to detection of a single entry of the test interface into a run-test idle state (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; Figure 1; and Figure 2); and

d. A decoder to receive the plurality of instructions for processing (Edgington column 3, lines 4-29).

9. Referring to claim 21, Edgington has taught an apparatus, including operating instructions residing on a machine-readable storage medium, for use in a device to handle a plurality of emulation instructions, the operating instructions causing the device to:

a. Load the plurality of emulation instructions into a single emulation instruction register (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; column 5, lines 25-29; column 6, lines 4-25; column 1, line 59 to column 11, line 11; Figure 1; Figure 2; Figure 5; and Figure 6). In regards

to Edgington, when the processor is in debug/test/emulator mode, all registers in the processor are used for the emulations instructions and data, so they are emulation registers.

b. Have a test interface enter a run-test idle state (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; Figure 1; and Figure 2);

c. Provide the plurality of emulation instructions to a processor in response to entry of the test interface into the run-test idle state (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; Figure 1; and Figure 2); and

d. Process the plurality of emulation instructions (Edgington column 3, lines 4-29).

10. Referring to claim 29, Edgington has taught an in-circuit emulator to monitor operations of the processor (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; Figure 1; and Figure 2).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 3, 5-8, 25, and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano, U.S. Patent Number 5,774,737 (herein referred to as Nakano) in view of Edgington et al., U.S. Patent Number 5,530,804 (herein referred to as Edgington).

13. Referring to claim 1, Nakano has taught a method comprising:

a. Loading the plurality of instructions into an instruction register (Nakano column 5, lines 25-29; column 6, lines 4-25; Figure 1; and Figure 2);

b. Receiving a plurality of instructions from the instruction register (Nakano column 5, lines 30-43; column 6, lines 4-25; column 7, lines 54-63; Figure 1; and Figure 2);

c. Determining a validity of a first instruction of the plurality of instructions by reading width bits in the first instruction (Nakano column 2, lines 37-40 and 63-65; column 9, lines 11-23; column 10, line 57 to column 11, line2; Figure 2; and Figure 5), the width bits which are read defining the validity and size of the first instruction (Nakano column 2, lines 37-40 and 63-65; column 9, lines 11-23; column 10, line 57 to column 11, line2; Figure 2; and Figure 5);

d. Providing the first instruction to a decoder of the processor if the first instruction is valid (Nakano column 5, lines 30-43; column 6, lines 4-25; column 7, lines 54-63; Figure 1; and Figure 2);

e. Without receiving a run-test idle state signal, determining validity of a second instruction of the plurality of instructions by reading width bits in the second instruction (Nakano column 2, lines 37-40 and 63-65; column 9, lines 11-23; column 10, line 57 to column 11, line2; Figure 2; and Figure 5), the width bits which are read defining the validity and size of the second instruction (Nakano column 2, lines 37-40 and 63-65; column 9, lines 11-23; column 10, line 57 to column 11, line2; Figure 2; and Figure 5); and

f. Providing the second instruction to the decoder if the second instruction is valid (Nakano column 5, lines 30-43; column 6, lines 4-25; column 7, lines 54-63; Figure 1; and Figure 2).

14. Nakano has not taught receiving a plurality of instructions from a test interface and emulation registers. Edgington has taught receiving a plurality of instructions from a test interface (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; Figure 1; and Figure 2) and emulation registers (Edgington column 1, line 63 to column 2, line 10). In regards to Edgington, when the processor is in debug/test/emulator mode, all registers in the processor are used for the emulations instructions and data, so they are emulation registers. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Edgington, allows for the system to be debugged and tested while not influencing normal operational state of the processor and at full operating clock frequency of the system (Edgington column 1, line 15-27 and column 3, line 4-16). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the debug/test/emulator mode of Edgington in the device of Nakano to test and debug the system while maintaining the current user operating state and at the system's full clock speed.

15. Referring to claim 3, Nakano in view of Edgington has taught storing the plurality of instructions in the emulation instruction register in subsequent clock cycles (Nakano column 5, lines 17-43; column 8, line 66 to column 9, line 9; Figure 1; and Figure 4).

16. Referring to claim 5. Nakano in view of Edgington has taught loading the plurality of instructions in parallel into the emulation instruction register (Nakano column 13, lines 53-67 and Figure 15).

17. Referring to claim 6, Nakano in view of Edgington has taught providing the second instruction to the decoder after the first instruction is completed (Nakano column 5, lines 17-43; column 6, lines 4-25; column 7, lines 54-63; column 8, line 66 to column 9, line 9; Figure 1; Figure 4; and Figure 2).

18. Referring to claim 7, Nakano in view of Edgington has taught providing the plurality of instructions to the decoder after a first run-test idle state without entering into a second run-test idle state (Edgington column 3, lines 4-29).

19. Referring to claim 8, Nakano in view of Edgington has taught providing the first and second instructions to a digital signal processor (Nakano column 5, line 44 to column 6, line 3 and Figure 1).

20. Referring to claim 25, Nakano in view of Edgington has taught wherein a pre-determined set of width bits indicates an instruction is invalid (Nakano column 2, lines 37-40 and 63-65; column 9, lines 11-23; column 10, line 57 to column 11, line2; Figure 2; and Figure 5).

21. Referring to claim 30, Nakano in view of Edgington has taught executing at least one of the plurality of instructions to monitor operation of the processor (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; Figure 1; and Figure 2).

22. Referring to claim 31, Nakano in view of Edgington has taught performing a debugging operation using the first and second instructions (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; Figure 1; and Figure 2).

23. Claims 11-15, 18-20, 23, 26, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edgington, as applied to claims 9, 16, and 21 above, in view of Nakano, U.S. Patent Number 5,774,737 (herein referred to as Nakano). Edgington has not taught

a. Determining a validity of each of the plurality of instructions before processing by reading bits in each instruction indicating a width of the instruction (Applicant's claims 11, 18, and 23).

b. Aborting processing of any invalid instructions and loading a next instruction into the emulation instruction register (Applicant's claims 12 and 18).

c. Loading a next instruction into the emulation instruction register if a no-operation instruction is loaded (Applicant's claims 13 and 19).

d. Providing the plurality of instructions to the processor a plurality of times without reloading the instruction register (Applicant's claim 14).

e. Providing the plurality of instructions to a digital signal processor (Applicant's claims 15 and 20).

f. Wherein the emulation instruction register comprises first and second registers (Applicant's claim 26).

g. A multiplexer to select between an instruction for the plurality of instructions to send to the processor pipeline (Applicant's claim 28).

24. Nakano has taught

a. Determining a validity of each of the plurality of instructions before processing by reading bits in each instruction indicating a width of the instruction (Applicant's

claims 11, 18, and 23) (Nakano column 2, lines 37-40 and 63-65; column 9, lines 11-23; column 10, line 57 to column 11, line2; Figure 2; and Figure 5).

b. Aborting processing of any invalid instructions and loading a next instruction into the emulation instruction register (Applicant's claims 12 and 18) (Nakano column 2, lines 37-40 and 63-65; column 9, lines 11-23; column 10, line 57 to column 11, line2; Figure 2; and Figure 5).

c. Loading a next instruction into the emulation instruction register if a no-operation instruction is loaded (Applicant's claims 13 and 19) (Nakano column 2, lines 37-40 and 63-65; column 9, lines 11-23; column 10, line 57 to column 11, line2; Figure 2; and Figure 5).

d. Providing the plurality of instructions to the processor a plurality of times without reloading the instruction register (Applicant's claim 14) (Nakano column 2, lines 37-40 and 63-65; column 9, lines 11-23; column 10, line 57 to column 11, line2; Figure 2; and Figure 5).

e. Providing the plurality of instructions to a digital signal processor (Applicant's claims 15 and 20) (Nakano column 5, line 44 to column 6, line 3 and Figure 1).

f. Wherein the emulation instruction register comprises first and second registers (Applicant's claim 26) (Nakano column 5, lines 25-29; column 6, lines 4-25; Figure 1; and Figure 2).

g. A multiplexer to select between an instruction for the plurality of instructions to send to the processor pipeline (Applicant's claim 28) (Nakano column 7, lines 38-53 and Figure 2).

25. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Nakano, that the VLIW system uses instruction memories more effectively, executes more instructions simultaneously, and has compatible with programs for conventional processors (Nakano column 1, line 63 to column 2, lines 11). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the VLIW system of Nakano in the device of Edgington to improve memory usage, instruction execution, and compatibility.

26. Claims 24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano in view of Edgington, as applied to claims 1 and 16 above, in view of Deao et al., U.S. Patent Number 5,970,241 (herein referred to as Deao). Nakano in view of Edgington has taught scanning instructions from an in-circuit emulator (ICE) to the test interface (Applicant's claim 24) (Edgington column 1, line 63 to column 2, line 10; column 3, lines 4-16; column 4, lines 40-50; Figure 1; and Figure 2). Nakano in view of Edgington has not taught the test interface comprising a Joint Test Action Group (JTAG) interface (Applicant's claim 24) and wherein the emulation control logic comprises a state machine (Applicant's claim 27). Deao has taught the test interface comprising a Joint Test Action Group (JTAG) interface (Applicant's claim 24) (Deao column 4, lines 11-18) and wherein the emulation control logic comprises a state machine (Applicant's claim 27) (Deao column 37, lines 39-53 and Figure 22). A person of ordinary skill in the art at the time the invention was made would have recognized that the JTAG test interface is an IEEE standard test interface and streamlines the testing scheme. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention as made to

incorporate the JTAG test interface of Deao in the device of Nakano in view of Edgington to streamline the testing scheme and meet IEEE standards.

Response to Arguments

27. Applicant's arguments with respect to claims 1, 3, 5-9, 11-16, 18-21, and 23-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
17 October 2005

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